IN THE CLAIMS

Please amend the following claims as presented, below, in clean-unmarked format:

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1. (Amended) An apparatus, comprising:

a first memory cell coupled to a first bit line and a second bit line;

a second memory cell coupled to a third bit line and a fourth bit line;

an address decoder coupled to the first and second memory cells to enable access to the first and second memory cells;

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a first comparator circuit coupled to the first and third bit lines to compare a voltage level on the first bit line with a voltage level on the third bit line at a time when data is output from the first memory cell on the first bit line and from the second memory cell on the third bit line; and

a second comparator circuit coupled to the second and fourth bit lines to compare a voltage level on the second bit line with a voltage level on the fourth bit line at a time when the complement of the data that is output on the first and third bit lines is output from the first memory cell on the second bit line and from the second memory cell on the fourth bit line.

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5. (Amended) The apparatus of claim 1, wherein the first comparator circuit is comprised of a single comparator with a first input coupled to the first bit line and a second input coupled to the third bit line, and

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wherein the second comparator circuit is comprised of a single comparator with a first input coupled to the second bit line and a second input coupled to the fourth bit line.

6. (Amended) The apparatus of claim 5, wherein the output of the first comparator is coupled to a first latch to store an indication that the voltage level on the first bit line differs substantially from the voltage level on the third bit line, and wherein the output of the second comparator is coupled to a second latch to store an indication that the voltage level on the second bit line differs substantially from the voltage level on the fourth bit line.

7. (Amended) The apparatus of claim 6, wherein the time at which the first and second latches are triggered is adjustable.

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8. (Amended) The apparatus of claim 6, wherein the first latch is a sticky latch that is triggered to latch an indication that the voltage level on the first bit line differs substantially from the voltage level on the third bit line, and wherein the second latch is a sticky latch that is triggered to latch an indication that the voltage on the third bit line differs substantially from the voltage on the fourth bit line.

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9. (Amended) The apparatus of claim 1, wherein the first and second comparator circuits are each comprised of:

a subtracting circuit with a first input coupled to the first bit line and a second input coupled to the second bit line;

a first comparator coupled to the output of the subtracting circuit; and

a second comparator coupled to the output of the subtracting circuit.

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14. (Amended) A method, comprising:

writing identical values to the first and second memory cells;

coupling a first memory cell to a first bit line;

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coupling the first memory cell to a second bit line;

coupling a second memory cell to a third bit line;

coupling the second memory cell to a fourth bit line;

coupling the first and third bit lines to inputs of a first comparator circuit;

coupling the second and fourth bit lines to inputs of a second comparator circuit;

reading the identical values from the first memory cell through the first bit line and from the second memory cell through the third bit line;

reading the identical values from the first memory cell through the second bit line and from the second memory cell through the fourth bit line that are complements of the values read through the first and third bit lines;

comparing the voltage levels on the first and third bit lines; and

comparing the voltage levels on the second and fourth bit lines.

15. (Amended) The method of claim 14, further comprising latching an indication from the first comparator circuit of whether or not the voltage level of the first bit line differs substantially from the voltage level of the third bit line, and latching an indication from the second comparator circuit of whether or not the voltage level of the second bit line differs substantially from the voltage level of the fourth bit line.

16. (Amended) The method of claim 14, further comprising setting the degree to which the difference in voltage levels between the first bit line and the third bit line, and between the second bit line and the fourth bit line are substantial.

[redacted]